1. (amended) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a well and an impurity region that is used to electrically connect a lower electrode of the capacitor element and another semiconductor element, wherein the well is located in the semiconductor substrate in the DRAM region, and the impurity region is located in the semiconductor substrate in the analog element region;

(b) simultaneously forming a storage node of the cell capacitor and the lower electrode of the capacitor element;

(c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

(d) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.

Please add new claims 17-29 as follows:

--17. (new) A method for manufacturing a semiconductor device including a semiconductor substrate having a DRAM region and an analog element region, comprising:

forming an impurity region in the analog element region of the semiconductor substrate;

forming an interlayer dielectric layer on the semiconductor substrate;

forming an embedded connection layer contacting the semiconductor substrate and extending through the interlayer dielectric layer;

forming a cell capacitor in the DRAM region and forming a capacitor element in the analog element region;

wherein the interlayer dielectric layer is positioned between the semiconductor substrate and the capacitor element;

wherein the embedded connection layer and the impurity region are positioned to electrically connect a lower electrode of the capacitor element to another semiconductor device element; and

wherein the embedded connection layer is positioned in a connection hole formed in the interlayer dielectric layer, with one end of the embedded connection layer connected to the lower electrode of the capacitor element at a bottom surface of the lower electrode of the capacitor element, and another end of the embedded connection layer connected to the impurity region.

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18. (new) A method according to claim 17, further comprising forming an additional capacitor element and additional embedded connection layer positioned in the analog element region so that the additional embedded connection layer extends from the additional capacitor element to the impurity region, and serially connecting the capacitor element and the additional capacitor element to each other through the impurity region.

19. (new) A method according to claim 17, further comprising forming a first resistance element and a second resistance element in the analog element region, and forming an impurity concentration of the first resistance element to be higher than an impurity concentration of the second resistance element so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

20. (new) A method according to claim 18, further comprising forming a first resistance element and a second resistance element in the analog element region, and forming an impurity concentration of the first resistance element to be higher than an impurity concentration of the second resistance element so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

21. (new) A method according to claim 17, further comprising forming a first resistance element and a second resistance element in the analog element region, and forming the first resistance element to include a silicide layer and forming the first resistance element to have a resistance value that is lower than a resistance value of the second resistance element.

22. (new) A method according to claim 18, further comprising forming a first resistance element and a second resistance element in the analog element region, and forming the first resistance element to include a silicide layer and forming the first resistance element to have a resistance value that is lower than a resistance value of the second resistance element.

23. (new) A method according to claim 17, further comprising forming a thickness of a dielectric layer of the capacitor element to be identical with a thickness of a dielectric layer of the cell capacitor.

24. (new) A method according to claim 18, further comprising forming a thickness of a dielectric layer of the capacitor element to be identical with a thickness of a dielectric layer of the cell capacitor.

25. (new) A method according to claim 19, further comprising forming a thickness of a dielectric layer of the capacitor element to be identical with a thickness of a dielectric layer of the cell capacitor.

26. (new) A method according to claim 21, further comprising forming a thickness of a dielectric layer of the capacitor element to be identical with a thickness of a dielectric layer of the cell capacitor.

27. (new) A method according to claim 18, further comprising forming an additional cell capacitor in the DRAM region.

28. (new) A method according to claim 27, further comprising forming a well in the DRAM region simultaneously with forming the impurity region in the analog element region.